HIGH PERFORMANCE DYNAMIC FEEDBACK CONTROL BASED STATIC RAM USING CNTFET TECHNOLOGY

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ABSTRACT

Performance of Static RAM is a major concern for VLSI researchers. Random-access memory (RAM) is a sort of PC or IC data stockpiling generally utilized for putting away run time factors and guidelines in microcontroller and handling units. It is most commonly used circuit in any part of memory-based devices. Technology scaling and short channel effects gives transition of work from MOSFET based to CNTFET based. CNTFET is proven to provide better performance in 22nm technology. In this paper, a special SRAM with Dynamic Feedback Control is proposed using CNTFET technology i.e. Carbon Nano Tubes Field Effect Transistor. The result shows improvement in Average Power Consumption, Speed, PDP, Leakage Current and Power Dissipation. The results are simulated on Synopsys HSPICE software tool.

Keywords: Dynamic Feedback Control; SRAM; 22nm; CNTFET

I. INTRODUCTION

Forcefully scaling the main supply voltage of SRAMs extraordinarily limits their dynamic and leakage power, a commanding segment in research for the power in present day ICs. [1] The power dissipation or consumption use can be limited using non-conventional device structures, new circuit topologies, and propelling the designing. Regardless of the way that, voltage scaling has provoked circuit activity in sub limit organization with least power use, anyway there is a downside of exponential diminishing in execution. [2] The standard activity in sub threshold limit is very troublesome in conventional SRAMs therefor the Dynamic Feedback Control based SRAM cells are gaining most importance in current research trends due to its high stability. [3] Thickness, power and execution are the basic parts required for these applications. Prior, those control to cutting edge rationale, which will be overpowered by unique power, has been lessened by cutting down those main voltages. [4] These advantageous structures need ultralow power consuming circuits to utilize battery for more term. The power use can be limited using

nonconventional IC structures, new circuit topologies, and propelling the building. Notwithstanding the way that, voltage scaling has incited circuit activity in sub limit organization with least power usage, anyway there is a disadvantage of exponential reducing in execution power. [5]

The power utilization by bit lines during composing is relative to the bit line capacitance, square of the bit line voltage and the recurrence of composing. There is a powerful approach in which the vitality put away in the bit line capacitance that is regularly lost to ground is gathered and siphoned once again into the source. This is known as vitality recuperation approach. Vitality put away in the bit lines is reused by the assistance of changes to neighboring piece lines so as to spare vitality in bit line charge-reuse strategy. This technique diminishes the swing voltages to a low swing voltage. In light of whether vitality reusing is done distinctly during composing cycle or during both composition and understanding cycles, there are variations. [6]

Notwithstanding recuperating the vitality from both bit lines the probability of working the SRAM cell with single b-line driven by an adiabatic driver is analyzed to reduce energy vitality. It is imperative to have low power and vitality proficient and stable SRAM which is basically utilized for on chip recollections. [7] Dynamic or exchanging power (PDYN) dissemination in SRAM is the charging/releasing power of bit lines and power devoured by the load circuits, for example, decoder what's more, and amplifiers. This effect is successfully reduced by the use of Dynamic Feedback Control in single ended SRAMs. [8]

Subsequently it is imperative to have low power and vitality proficient and stable SRAM which is mostly utilized for on chip recollections. There are different methodologies that are received to lessen power dispersal, similar to plan of circuits with power supply voltage scaling, power gating and sleep mode-based technique. Lower power supply voltage lessens the dynamic power in quadratic design and spillage/leakage power in an exponential way. [9]

To continue the superior of the circuit structure and defeat the scaling silicon channel difficulties, the ongoing inquiries about will in general substitute a traditional channel material for transistors with new nano-materials that have very crucial physical and electrical properties contrasted with MOS, such carbon nano-cylinder, Carbon Nano tubes, to work at low voltage with a low sub-limit incline. In this manner, CNTFET are misused as a powerful transistor in advanced rationale applications rather than MOS partner particularly the low power application. [10]

II. PROPOSED WORK

This section proposes the circuit for 8T SRAM with dynamic feedback control in CNTFET 22nm. The circuit consists of all CNTFETs and power is 0.7v. The circuit is shown in Figure 1. This circuit using the SPICE model of CNTFET is implemented on HSPICE by the use of node coding for each

transistor. After which a transient analysis is performed on the circuit for proper analysis. There are basically three modes for the SRAM working which are Read, Write and Hold Mode. The circuit is tested in all modes for proper analysis. The transient analysis performed in the circuit is from 1ns to 40ns. The calculated performance metrics are Average Power Consumption, Delay, Power Dissipation, PDP (Power Delay Product) and Leakage Current.

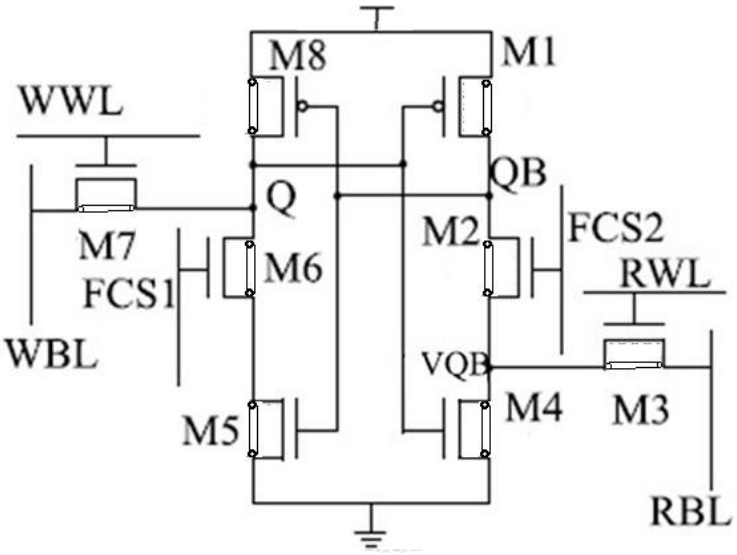

Figure 1: Proposed SRAM 8T using CNTFET with Dynamic Feedback Control

III. RESULTS

In table 1, the simulations results are shown between proposed work and existing work.

Table 1: Simulation results

	SRAM 8T DFC MOS	SRAM 8T DFC PROPOSED CNTFET
Average Power Consumption(W)	7.11E-08	6.75E-08
Delay(S)	2.50E-10	1.75E-10
Power Dissipation(W)	3.23E-09	1.39E-10
PDP(J)	8.06E-19	2.45E-20
Leakage Current(A)	2.54E-09	1.18E-10

In figure 2, the result comparison of Average power consumption is shown. It shows that performance of proposed circuit is increased with the use of CNTFET technology.

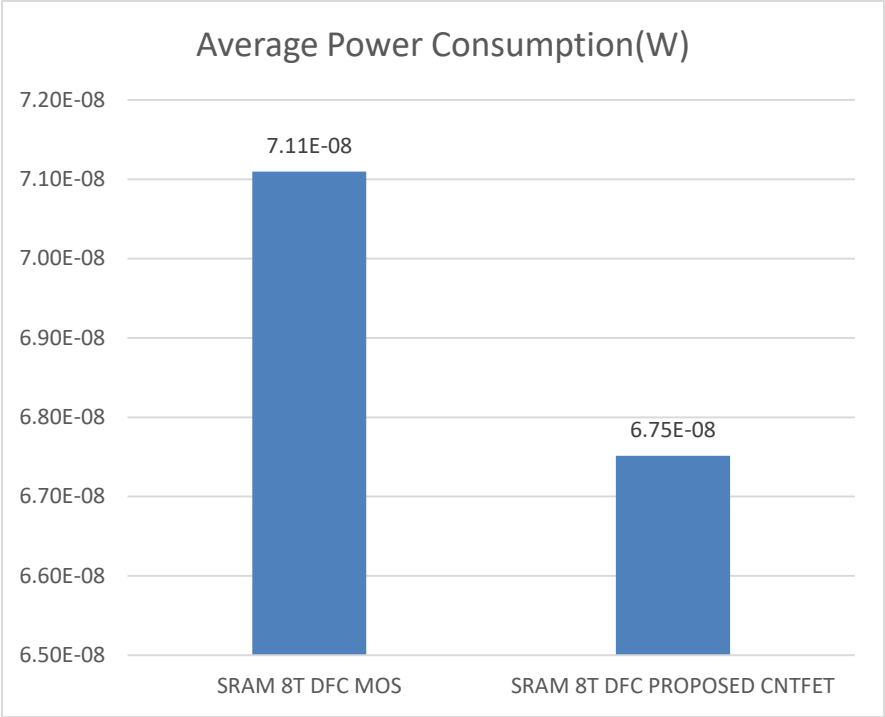

Figure 2: Result for SRAM DFC Average Power

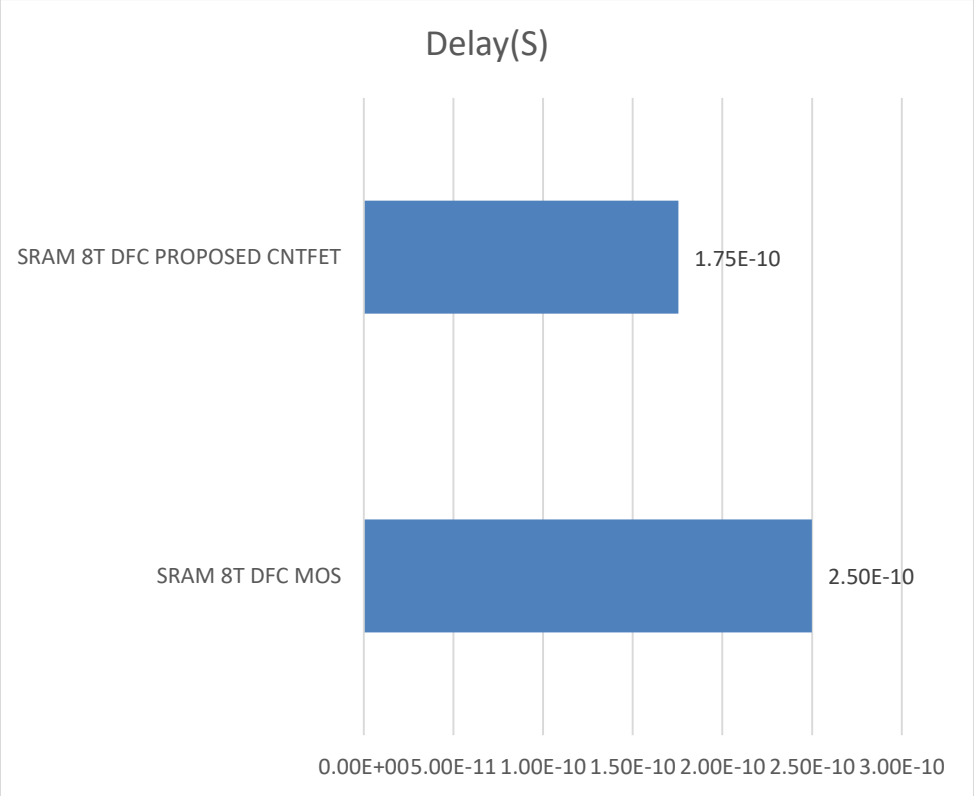

Figure 3: Result for SRAM DFC Delay

In figure 3, delay comparison in seconds is shown, for proposed work is very high speed.

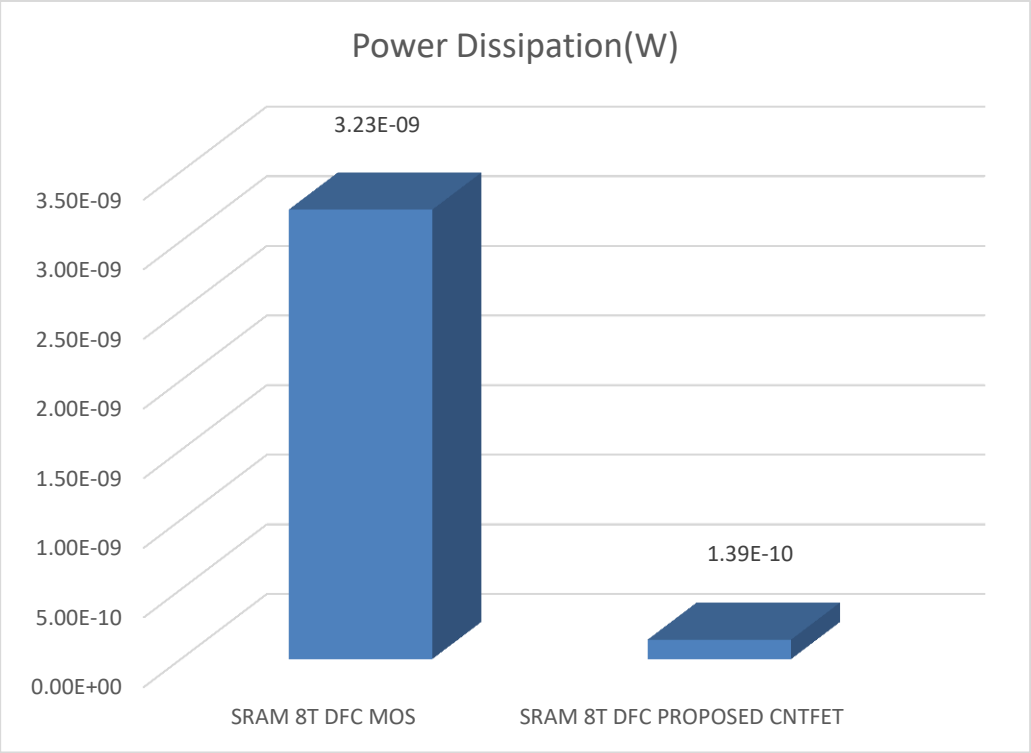

Figure 4: Result for SRAM DFC Power Dissipation

In figure 4, the power dissipation result is shown for proposed CNTFET based Dynamic Feedback Control Static Ram.

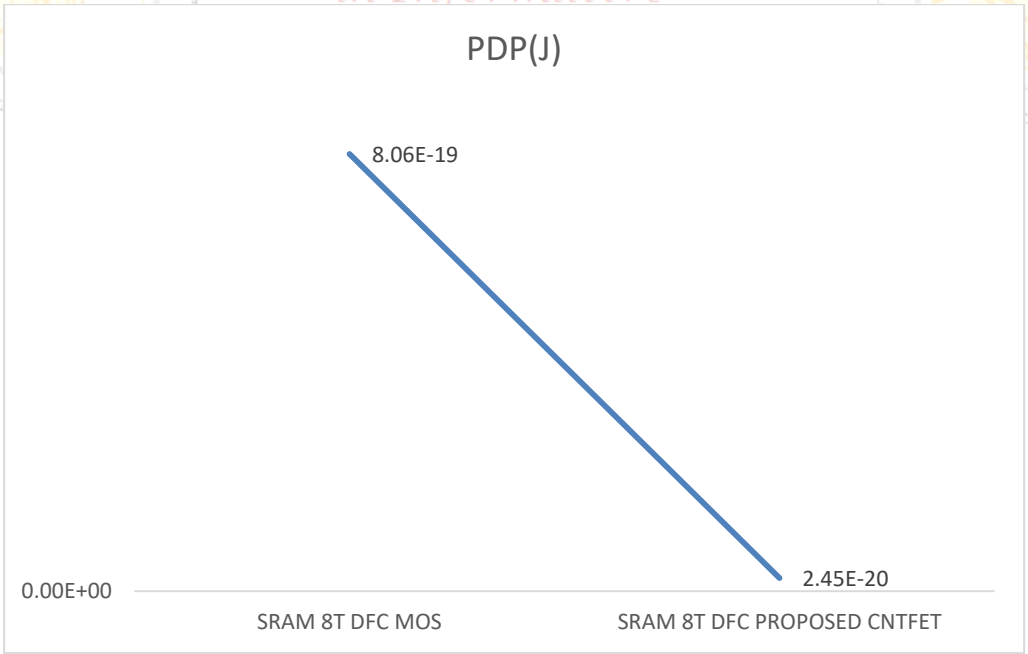

Figure 5: Result for SRAM DFC PDP

PDP or power delay product is important factor to calculate the performance which is minimum in case of proposed work as shown in figure 5. Leakage Current performance for CNTFET based SRAM DFC is shown in Figure 6.

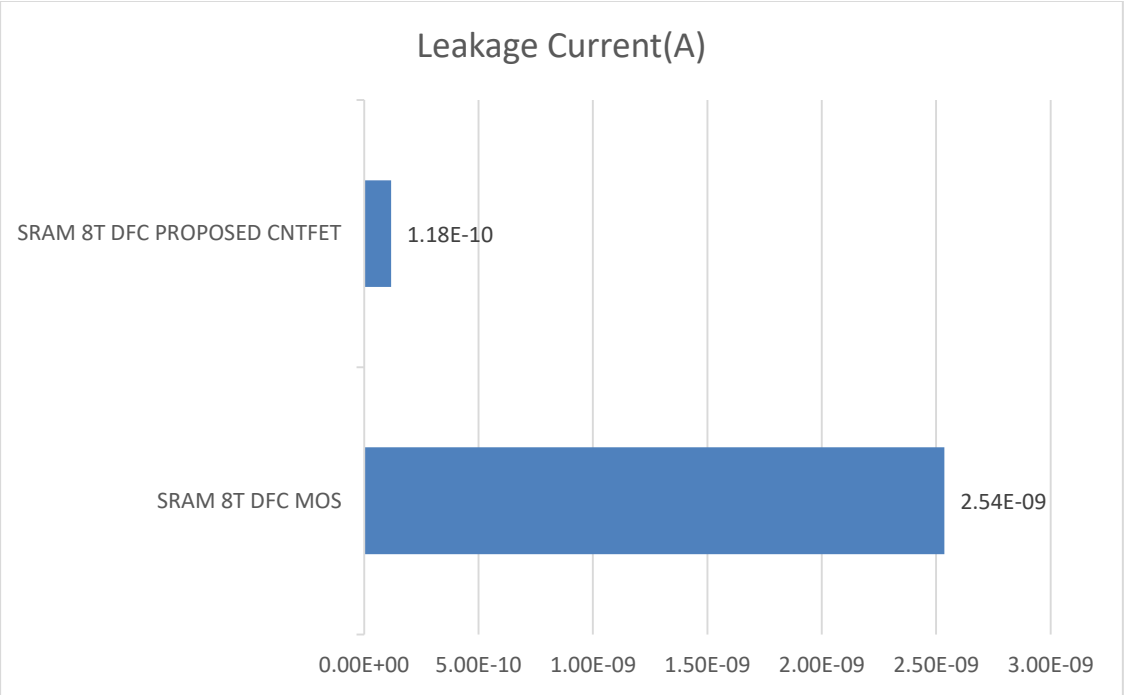

Figure 6: Result for SRAM DFC Leakage Current

The output waveform in Write mode is shown in Figure 7.

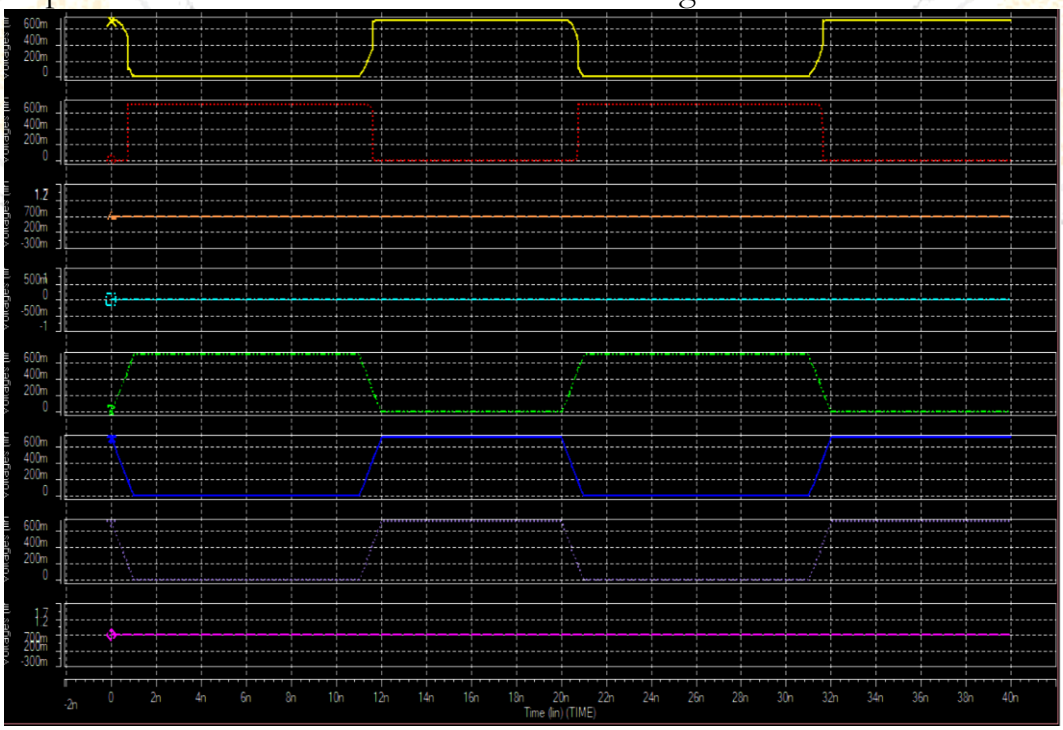

Figure 7: CNTFET based Output Waveform for SRAM DFC

IV. CONCLUSION

This technology scaling has provided us with increased circuit performance over the past two decades. The industry has scaled the conventional transistors for the past six years using several innovative techniques such as high-k dielectrics and strained silicon. However, scaling of conventional transistors beyond the 22nm node is very difficult due to short-channel effects, such as drain-induced barrier lowering (DIBL), sub threshold slope and sub threshold leakage current. DGFETs have emerged as a possible solution to continue technology scaling. In this work, the results of SRAM based CNTFET in Dynamic Feedback Control shows better response for power and delay and hence its performance is improved.

REFRENCES

[1] C. B. Kushwah, Student Member, IEEE and S. K. Vishvakarma, Member, IEEE" A Single-Ended with Dynamic Feedback Control 8T Subthreshold SRAM Cell," IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 24, Issue 1, pp 373-377, 2016.

[2] Chandramauleshwar Roy, Aminul Islam, "Characterization of single-ended 9T SRAM cell", Microsystem Technologies, Vol.26, pp 1591-1604, 2020.

[3] M.N. Naga Vyshnavi, S. Mohan Das, "Design of Energy Efficient 8T SRAM cell at 90nm Technology", International Research Journal of Engineering and Technology (IRJET), Volume: 06, Issue: 02, Feb 2019.

[4] S Renukarani, Bhavana Godavarthi, Sk Bia Roshini, Mohammad Khadir," A Novel concept on 8-Transistor Dynamic Feedback Control on Static RAM Cell Array " International Journal of Engineering & Technology, vol.7, Part 2.20, pp 109-113 ,2018.

[5] Motla Sushma, Mr.B.Kishore Kumar, "A Single-Ended with Dynamic Feedback Control 10T Subthreshold SRAM Cell", International Journal of Management, Technology and Engineering, Volume 8, Issue XII, pp 5562-5569, December 2018.

[6] Devarapalli Mounika, Akondi Narayana Kiran, "Implementation of Low Power 8T SRAM Cell with Dynamic Feedback Control using AVLG Technique", Int. Journal of Engineering Research and Application, Vol. 7, Issue 11, (Part -3), pp.82-85, November 2017,.

[7] Aisha Mobeen Mohammad, P.Lakshmi, M.Basha, "Sub Threshold SRAM Cell with a Single-Ended Dynamic Feedback Control 8T", Vol 3, Issue 9, 2016.

[8] K.M. Santhoshi Priya, K. Prasad Babu, S. Ahmed Basha, K.Sudhakar, "Design of Ultra Low Power SRAM Cell", International Journal of Advanced Research in Science, Engineering and Technology, Vol. 4, Issue 2 , February 2017.

[9] Athira M R and Anu Thankam George, "Sub threshold 8T SRAM Cell with Dynamic Feedback", National Conference on Recent Trends in VLSI, Communication and Networks 2018 (RTVCN2K18) Vol 4, Issue 5, 2018.

[10] Sonal Verma1, Ravi Tiwari, "Single Ended 8T Subthreshold SRAM Cell for

Dynamic Feedback Control Signal", International Journal for Research in Applied Science & Engineering Technology, Volume 6, Issue III, March 2018.

[11] PRAVEENA KUMARI et.al, "Design and Analysis of 16bit Ripple Carry Adder and Carry Skip Adder Using Graphene Nano Ribbon Field Effect Transistor (GNRFET)" International Journal of Innovative Science and Research Technology, Volume 2, Issue 7, July– 2017.

[12] Preetika Sharma et.al, "Effect of temperature on the conductance of GNRFET", NCTP-09, April 2016.

[13] Huei Chaeng Chin et.al, "Enhanced Device and Circuit-Level Performance Benchmarking of Graphene Nanoribbon Field-Effect Transistor against a Nano-MOSFET with Interconnects" Hindawi Publishing Corporation, Journal of Nanomaterials, Volume 2014.

[14] Amit Sangalet.al,"GNRFET as future low power devices", ISLEPD, September 2013.

[15] Iraj Sadegh Amiri, Mahdiar Ghadiry "Analytical Modelling of Breakdown Effect in Graphene Nanoribbon Field Effect Transistor," Applied Sciences and Technology-Springer publisher, 2017.