Design and Performance Analysis of Inverter Using ECRL, MERL and PFAL

Raman
Department of Electronics & Communication Engineering, Guru Jambheshwar University of Science & Technology, Hisar, India

Ramnish Kumar
Asst. Prof. Department of Electronics & Communication Engineering, Guru Jambheshwar University of Science & Technology, Hisar, India

Abstract

In this paper, different low energy design techniques are analyzed to overcome the shortcoming of traditional circuits. An inverter circuit is used as a reference circuits to compare three adiabatic logic designs like ECRL, MERL and PFAL. The ECRL, MERL and PFAL designed inverter circuits are simulated by using mentor graphics VLSI design software Pyxis _v10.5_5_201606075 and the obtained results are compared in terms of rise time, fall time, transistor count, delay, slew rate etc. Finally, I calculated the delays, Slew rate and other parameter of PFAL based circuit results better as compared to ECRL and MERL.

Keywords: *Inverter, ECRL, MERL, PFAL, Adiabatic Switching.*

1. Introduction

Over the last few decades, a continuous development in IC device technology in which circuit density is increased by decreasing feature size. The operating voltage is also being reduced to keep limit in energy dissipation density. As a result of reduction in energy dissipation enable a device to consume less energy. This less energy consumption and energy dissipation reduction make device more reliable. To make more reliable device researcher will consider the energy budget logic circuits, omitting for now the display and other energy or power hungry component [1]. It is necessary to find suitable adiabatic computing is to construct circuits that allow each required electron to be collected from minimum voltage limit and transferred to the maximum voltage limit [2].

It is with this in mind, that three possible methods (or logic) of decreasing dynamic power dissipation, ECRL, MERL and PFAL based inverters are investigated by means of simulation techniques. The interest growing in low power logic circuitry is to increase battery life in portable device and to reduce the cooling requirement of complex IC. To fulfill these requirement proposed three adiabatic logic topologies minimize dissipation by keeping the voltage across conducting devices small at all times [3].

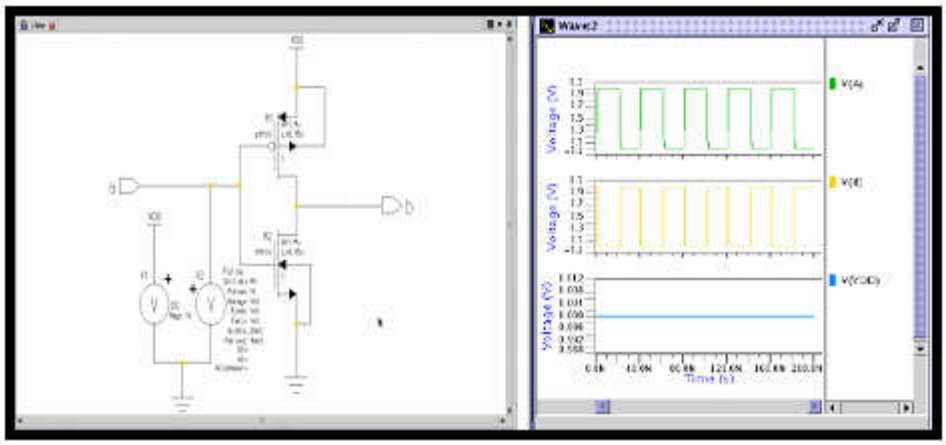

Fig.1.1 Conventional CMOS Inverter Circuit and its Simulated Waveform

Here a new question arose in my mind, why an inverter circuit is used? It is because inverter circuit is used for analysis of all digital design because its designing, operation and properties are clearly understood. Hence, these three adiabatic logic (ECRL, MERL and PFAL) inverter analysis help to explain behavior of complex integrated circuits. Method for power reduction depending upon the application of techniques to VLSI circuits has recently come under renewed investigation [4]. The one that motivated with this investigation were analysis of energy recovery logic. For low energy dissipation it is necessary to operate a circuit in an adiabatic regime. In adiabatic

circuit energy used to charge the capacitive nodes in a circuit and during discharge it may be recovered or stored for reuse [5]. As shown in Fig 1.1 conventional CMOS circuits are non-adiabatic. In these circuits capacitive node are quickly charged and discharged through MOS device.

Energy recovery technique originally developed for low-power digital circuits. All three proposed logic are useful for energy recovery because each one capable to recycle the energy from capacitance in each cycle of clock. I am investigating performance at various parameter impacts on these to find better one. The comparison of different parameter variations against different energy recovery techniques (ECRL, MERL and PFAL) so we get which one are applied to real life application to demonstrate their low power high performance properties.

2. Different Energy Recovery Logic Circuits

2.1 Efficient Charge Recovery Inverter Logic

The basic operation of ECRL inverter with schematic shown in Fig 2.1 and its schematic based on Differential Cascade Voltage Switch Logic which reduces coupling effect [6]. ECRL circuit and 2N2N-2P logic circuit are approximately same but two cross coupled N-MOS in 2N2N-2P logic is more than ECRL logic [7].

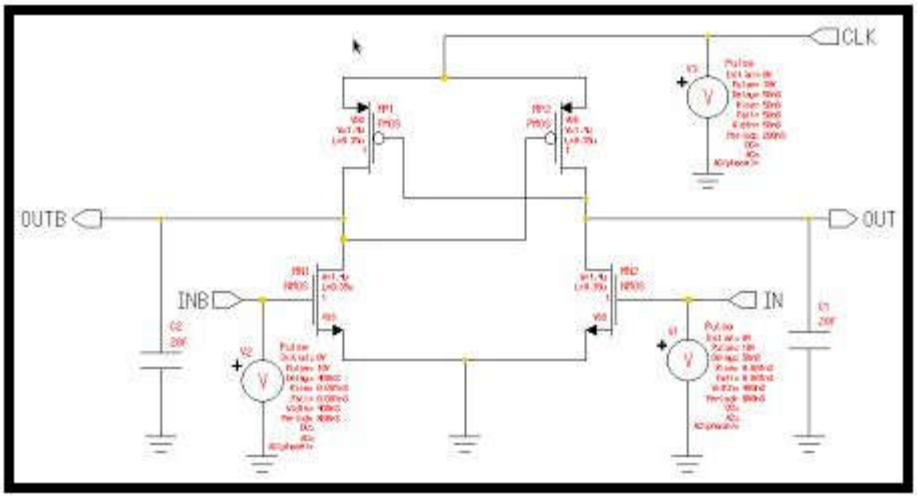

Fig.2.1 Schematic of ECRL inverter

Working of ECRL based inverter is same as conventional inverter. Simulated output waveform shown in Fig 2.2 and

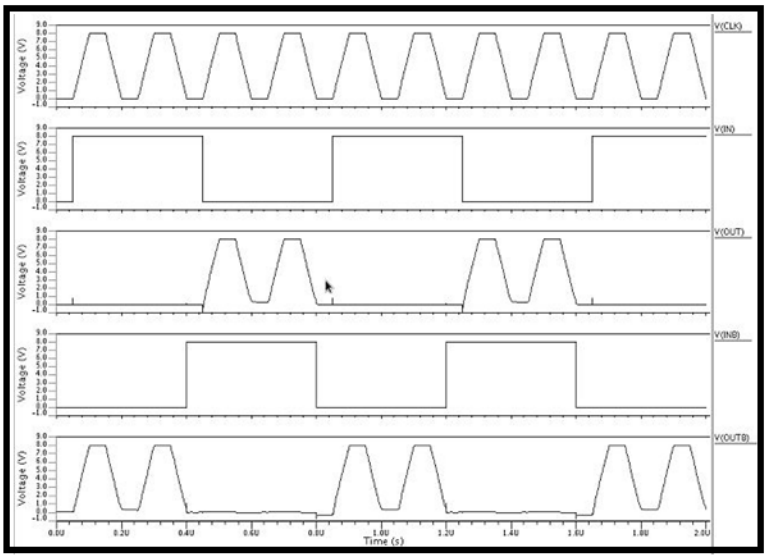

Fig.2.2 Simulated Waveform of the ECRL Inverter

ECRL based inverter is design and simulates in Mentor Graphic VLSI design software Pyxis _v10.5_5_201606075. The transient analysis with pulse voltage source, capacitive load is of 20f. In ECRL inverter designing, we use 2PMOS and 2 NMOS. All function of inverter is performed by NMOS while PMOS work as a pull-up network for performance analysis at different voltage its Frequency, Rise time, Fall time, Duty cycle, Settle time, Overshoot, Period, Undershoot, Pulse width, Slew rate.

2.2 Modified Energy Recovery Logic Inverter Circuit

The Modified Energy Recovery Logic (MERL) based inverter is design and simulates in Mentor Graphic Software of Pyxis _v10.5_5_201606075.The basic operation of MERL inverter with schematic shown in Fig 2.3.

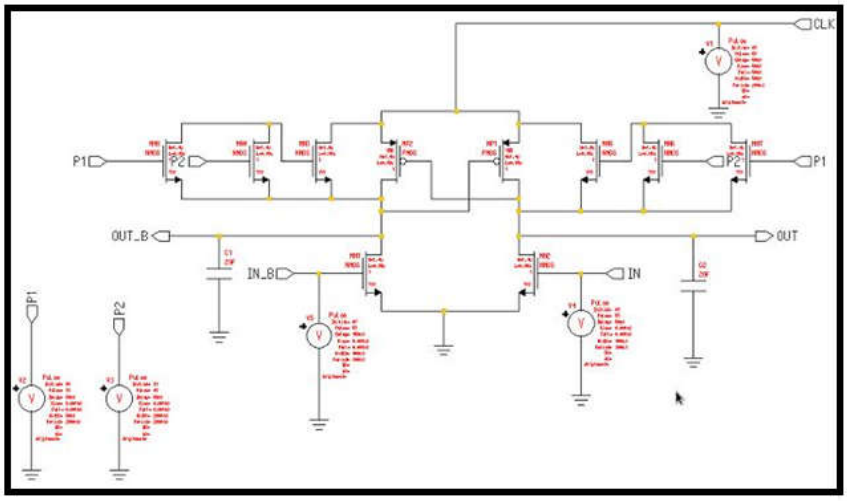

Fig.2.3 Schematic of MERL inverter

In this software Pyxis language interface is used for output compilation. The transient analysis with pulse voltage source, capacitive load of 20f .The MERL based inverter; we used 2- PMOS, 8-NMOS, 5-Pulse voltage source. Out of these voltage source each one have different configuration. The drain of MP1 is out terminal and drain of MP2 is out_ bar terminal. The Simulation result of MERL based inverter is shown in Fig.2.4.

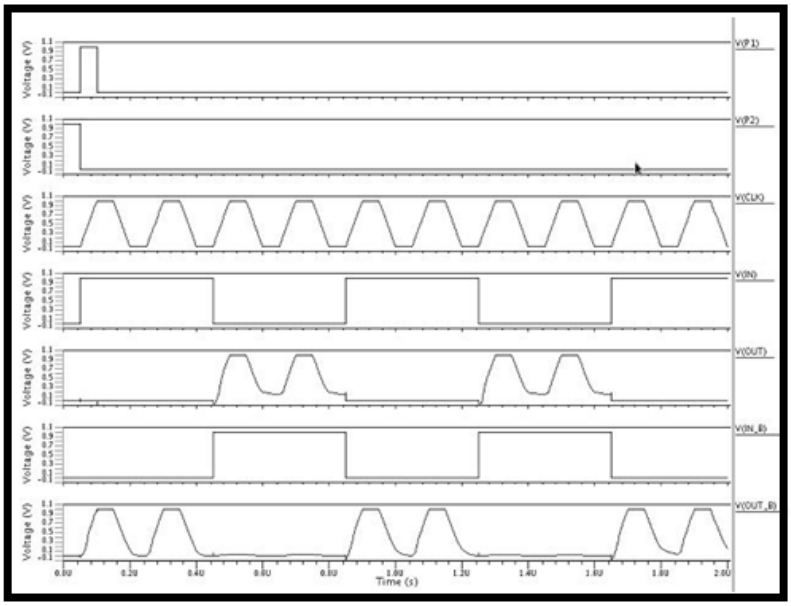

Fig.2.4 Simulated waveform of the MERL inverter

In this figure, first two are supply pulse voltage, third one is CLK input V[CLK], fourth and fifth is input V[IN] and output V[OUT], sixth is input bar V[IN_B] seventh one is output bar V[OUT_B]. MERL based inverter circuits overcome difficulty arise in ECRL based circuits but its designing is complex as compared to ECRL circuits. Transistor count of MERL is much larger than ECRL. MERL circuit simulation and trouble shooting is very difficult due to its complexity.

2.3 Positive-Feedback Adiabatic Logic Inverter Circuit:

PFAL stands for "Positive Feedback Adiabatic Logic". It is called positive feedback because; Positive feedback from either of the N-trees is needed to obtain the full swing of output.

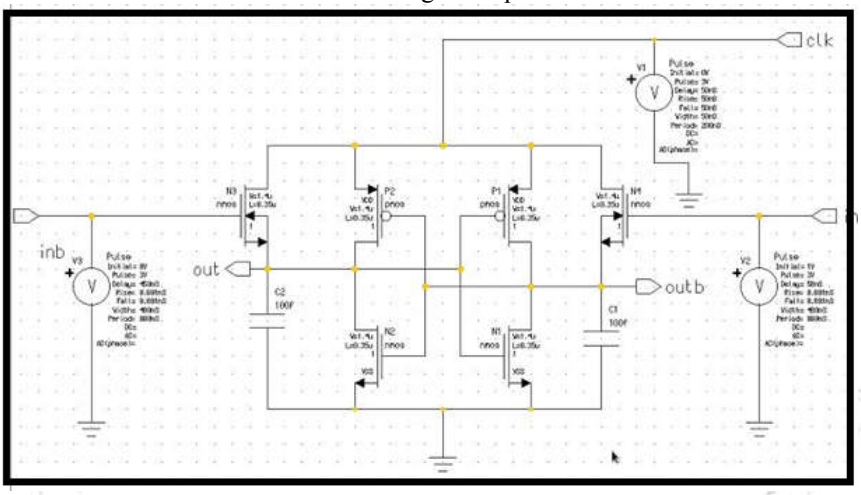

Fig.2.5 Schematic of PFAL inverter

PFAL circuits consist of an adiabatic amplifier, a latch made of two P-MOS and two N-MOS, avoids a logic level degradation on the output nodes out and out b. The schematic and simulation result of PFAL Inverter are shown in Fig.2.5 and Fig.2.6 respectively.

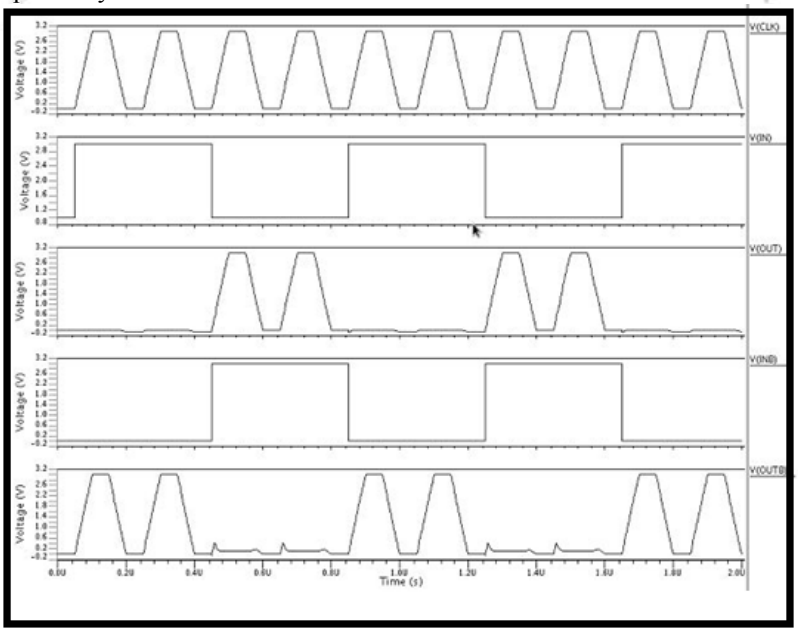

Fig.2.6 Simulated waveform of the PFAL inverter

PFAL based inverter is design and simulates in Mentor Graphic Software of Pyxis _v10.5_5_201606075.The PFAL based inverter we used 2- PMOS, 4-NMOS, 3-Pulse voltage source. In this figure first is supply CLK voltage

V[CLK], second is input V[IN], third and fourth is output V[OUT] and input bar V[INB], fifth is output bar V[OUTB]. After comparison between ECRL, MERL and PFAL based inverter circuits I found that designing of PFAL is complex as compared to ECRL circuits but simple as compared to MERL. Transistor count of PFAL is larger than ECRL but less than MERL. PFAL circuit simulation and trouble shooting is difficult than ECRL but easy than MERL circuit due to its complexity.

3. Results and Discussion

3.1 ECRL INVERTER

Table 3.1, shows that at 1V, The ECRL inverter frequency is 1.2510 MHz, Pulse width is 300.48ns, Slew rate is 25.779 MEG, and Period is 799.36ns. But when voltage is increased to 2V, The ECRL inverter frequency is 5.0036 MHz, Pulse width is 99.882ns, Slew rate is 46.060 MEG, Period is 199.86ns and similarly as so on.

Table 3.1: Simulation result of ECRL based Inverter

Sr. No.	Voltage	Freqency (MHz)	R_Time (ns)	F_Time (ns)	D_Cycle (M)	S_Time (Us)	O_shoot (MV)	Period (ns)	U_shoot (MV)	P_Width (ns)	S_Rate (MEG)
1	1V	1.2510	32.979	63.380	375.90	1.6500	662.14uv	799.36	522.10UV	300.48	25.779
2	2V	5.0036	36.913	62.926	499.77	1.6500	730.89UV	199.86	215.37MV	99.882	46.060
3	3V	5.0014	39.839	47.709	499.89	1.6500	118.64NV	199.94	1.4431MV	99.949	64.011
4	4V	4.9984	40.220	44.761	500.27	1.6500	101.23NV	200.06	453.52MV	100.09	84.537
5	5V	4.9991	40.468	44.665	500.74	1.6500	99.479NV	200.04	561.26MV	100.17	105.02
6	6V	5.0011	41.196	45.684	499.87	1.6500	90.530NV	199.95	4.9506MV	99.951	123.79
7	7V	5.0004	41.676	45.431	499.94	1.6500	21.865NV	199.98	5.5245MV	99.980	142.76
8	8V	5.000	42.082	44.064	500.05	1.6500	3.1772NV	200.00	4.0536MV	100.01	161.60
9	9V	4.9997	42.227	44.530	500.06	1.6500	700.45PV	200.01	1.7997MV	100.02	181.18
10	10V	5.000	42.365	44.572	500.01	1.6500	8.2049NV	200.00	1.3352MV	100.00	200.64

3.2 PFAL INVERTER

Table 3.2, shows, at 1V, PFAL inverter frequency is 5.0017 MHz, Pulse width is 100.01 ns, Slew rate is 19.841 MEG and Period is 199.93ns.But when voltage is increased to 2V, PFAL inverter frequency is 5.0000 MHz, Pulse Width is 99.991ns, Slew rate is 39.829 MEG, Period is 200.00ns.

Table 3.2: Simulation result of PFAL based Inverter

Sr No.	Voltage	Freqency (MHz)	R_Time (Ns)	F_Time (Ns)	D_Cycle (M)	S_Time (Us)	O_shoot (MV)	Period (Ns)	U_shoot (MV)	P_Width (Ns)	S_Rate (MEG)
1	1V	5.0017	42.843	42.501	500.23	1.5987	10.951NV	199.93	23.019MV	100.01	19.841
2	2V	5.0000	42.678	42.342	499.96	1.5987	618.07NV	200.00	138.46UV	99.991	39.829
3	3V	5.0000	42.598	42.464	500.05	1.5982	1.0569UV	200.00	81.210MV	100.01	59.865
4	4V	5.0000	42.554	42.505	500.01	1.5975	94.149NV	200.00	111.52MV	100.00	79.900
5	5V	4.9999	42.517	42.502	500.01	1.5981	46.824NV	200.00	142.41MV	100.00	99.952
6	6V	5.0000	42.474	42.517	499.99	1.5986	98.112NV	200.00	173.27MV	99.998	120.06
7	7V	5.0000	42.461	42.513	500.01	1.5976	175.12NV	200.00	203.72MV	100.00	140.12
8	8V	4.9999	42.443	42.534	500.01	1.5976	234.92NV	200.00	534.83MV	100.00	160.19
9	9V	5.0000	42.432	42.551	500.01	1.5976	39.695NV	200.00	265.14MV	100.00	180.25
10	10V	5.0000	42.428	42.559	500.03	1.5983	526.81NV	200.00	294.62MV	100.00	200.28

3.2 MERL INVERTER

Table 3.3 shows, at 1V the MERL inverter frequency is obtained as 1.2511 MHz, Pulse width is 300.56ns, Slew rate is 26.003 MEG, and Period is 799.29 ns. But when voltage is increased to 2V, The MERL inverter frequency is 5.0038 MHz, Pulse width is 99.859 ns, Slew rate is 46.07 MEG, Period is 199.85ns and similarly as so on.

Table 3.3: Simulation Result of MERL Based Inverter

Sr. No.	Voltage	Freqency (MHz)	R_Time (ns)	F_Time (ns)	D_Cycle (M)	S_Time (Us)	O_shoot (MV)	Period (ns)	U_shoot (MV)	P_Width (ns)	S_Rate (MEG)
1	1V	1.2511	32.685	97.485	376.03	1.6501	93.297UV	799.29	67.351	300.56	26.003
2	2V	5.0038	36.896	64.348	499.68	1.65	1.1552MV	199.85	172.5	99.859	46.07
3	3V	5.0015	39.585	48.048	499.86	1.65	106.64NV	199.94	300.01	99.942	64.412
4	4V	5.0009	40.157	46.581	499.9	1.65	214.70NV	199.96	398.93	99.962	84.662
5	5V	5.0017	40.41	44.044	499.82	1.65	464.10UV	199.93	1.8395	99.93	105.18
6	6V	5	41.252	44.215	500.09	1.65	48.402NV	200	660.95UV	100.02	123.64
7	7V	4.9995	41.665	45.048	500.08	1.65	13.818NV	200.02	514.92UV	100.02	142.81
8	8V	5.0006	41.834	43.882	499.93	1.65	416.04NV	199.98	637.90MV	99.974	162.55
9	9V	5.0001	42.184	44.98	499.99	1.65	50.530NV	199.99	1.0816MV	99.994	181.36
10	10V	4.9999	42.192	44.859	499.97	1.65	129.14NV	200	2.0007MV	99.996	201.46

Table 3.4: Delay of ECRL, MERL, PFAL Based Inverter at Different Voltage

Sr. No.	Voltage	ECRL Delay (ns)	MERL Delay (ns)	PFAL Delay (ns)
1	1V	374.52	374.32	174.63
2	2V	174.93	174.88	174.86
3	3V	174.93	174.92	174.93
4	4V	174.94	174.93	174.94
5	5V	174.95	174.94	174.94
6	6V	174.96	174.95	174.94
7	7V	174.96	174.96	174.95
8	8V	174.97	174.96	174.95
9	9V	174.97	174.96	174.95
10	10V	174.97	174.96	174.95

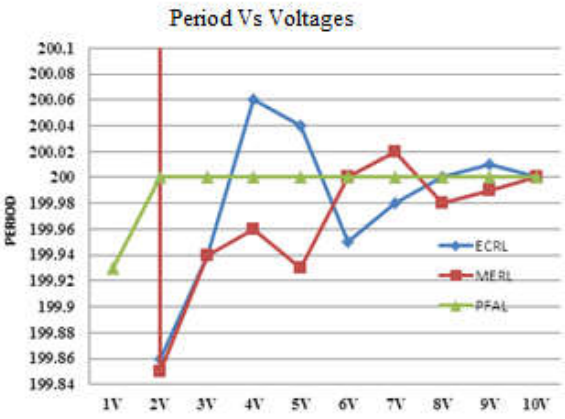

Fig.3.1: Period Vs Voltage Graph of ECRL, MERL and PFAL Inverter

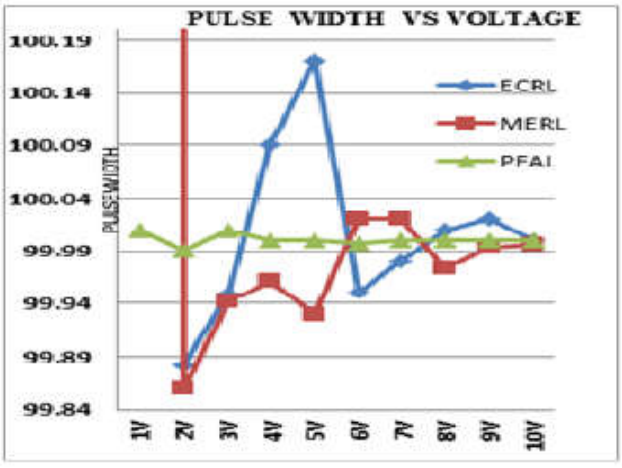

Fig.3.2: Delay Vs Voltage Graph of ECRL, MERL and PFAL

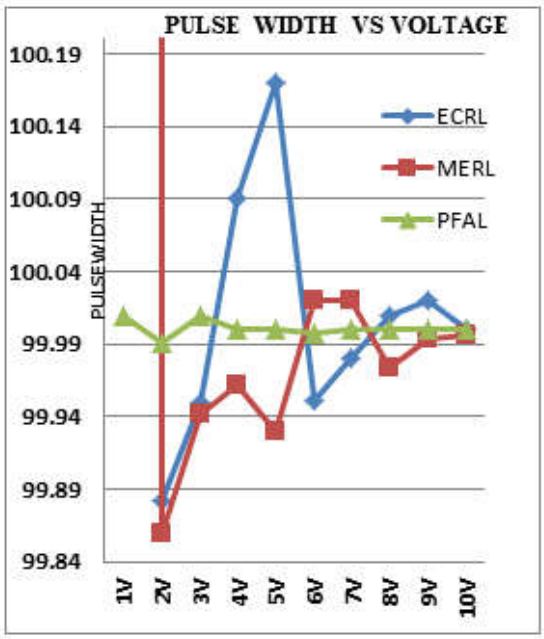

Fig.3.3: Pulse Width Vs Voltage Graph of ECRL, MERL and PFAL

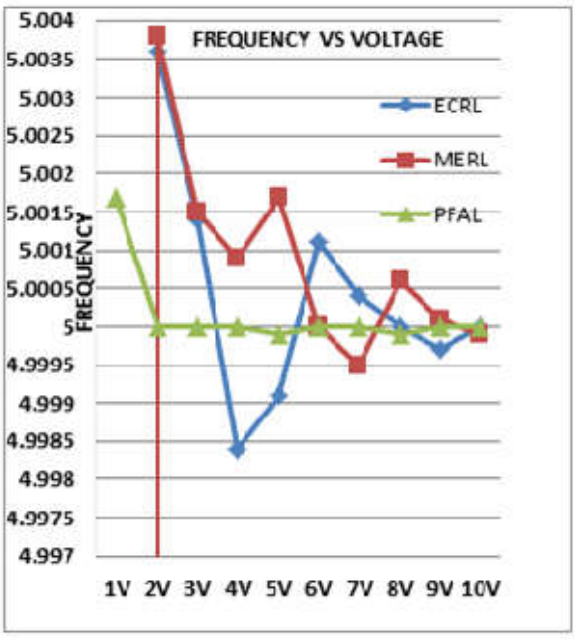

Fig.3.4: Frequency's Voltage Graph of ECRL, MERL and PFAL

4. Conclusion

Inverter circuits have been implemented using ECRL, MERL and PFAL techniques and these three techniques are compared w.r.t. transistor count, maximum operating frequency, pulse width, slew rate, delay, duty cycle, period etc. From the results and observation, it is found that the transistor count of MERL inverter is higher than ECRL and PFAL. PFAL Inverter Period and Frequency w. r. t Voltage is consistent as compared to ECRL Inverter and MERL Inverter, PFAL Inverter Slew rate, Pulse width, Delay and Settle time and w. r. t voltage is smaller as compared to ECRL Inverter. MERL Inverter, PFAL Inverter Duty cycle w. r. to Voltage is greater than ECRL Inverter and MERL Inverter. PFAL inverter Frequency, Pulse Width, Slew rate, Period with respect to voltage is better than ECRL and MERL. The output levels for PFAL are better and stabilize as compared to ECRL and MERL based inverter but the transistor count of PFAL based is higher than ECRL but less than MERL.

References

[1] J. S. Denker "A review of adiabatic computing" IEEE Symposium on Low Power Electronics, pp. 94-97, 1994.

[2] A. Gamer, J. S. Denker, S. C. Avery, A. G. Dickinson and T. R. Wik, "Adiabatic computing with the 2N-2N2D logic family," IEEE Symposium on VLSI Circuits Digest of Technical Papers, pp.25-26,June 1994.

[3] R. T. Hmxnan and M.F.Schlecht, "Power dissipation measurements on recovered energy logic," IEEE Symposium on VLSI Circuits Digest of Technical Papers, pp. 19-20, June 1994.

[4] A. P. Chandrakasan and R. W. Brodersen "Minimizing Power Consumption in Digital CMOS Circuits" Proceedings Of The IEEE, Vol.83, No. 4, April 1995.

[5] A.G. Dickinson and J.S. Denker, "Adiabatic Dynamic Logic," IEEE Solid-Circuit, vol.30, pp. 311-315, Mar-1995.

[6] Yong Moon and Deog-Kyoon Jeong "Efficient Charge Recovery Logic" IEEE journal of solid-state circuits, pp. 129-130, 1995.

[7] Yong Moon and Deog-Kyoon Jeong, "An efficient charge recovery logic circuit," IEEE Journal of solid-state circuits, vol. 31, pp. 514-522, April 1996.

[8] Samik Samanta, "Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSI-EDA Tool," in IJCCT,Vol.2,3rd-5th December 2010.

[9] Jianying Shi, Baozeng Guo, Rui Zhao, "Design of the Modified Energy Recovery Logic Circuit," in IEEE-2011.
[10] R.K. Yadav, A. K. Rana, ShwetaChauhan, Deepesh Ranka and Kamalesh Yadav, "Adiabatic Technique For Energy Efficient Logic Circuits Design," in IEEE 2011.
[11] Arun Kumar and Manoj Sharma,"Design and Analysis of MUX using Adiabatic Techniques ECRL and PFAL," in IEEE-2013.
[12] A. K. Bakshi and Manoj Sharma, "Design of Basic Gates Using ECRL and PFAL," in IEEE-2013.
[13] Sakshi Goyal, Gurvinder Singh and Pushpinder Sharma, "Variation of Power Dissipation for Adiabatic CMOS and Conventional CMOS Digital Circuit," in IEEE-2015.
[14] M. L. Keote and Dr. P. T. Karule, "Design and Implementation of Energy Efficient Adiabatic ECRL and Basic Gates," in IEEE-2015.
[15] A.K. Lenka, K. R. Behera, P. Karmakar, "A Comparative Analysis of NMOS and PMOS used in 180nm Process CMOS Inverter," in IEEE-2018.